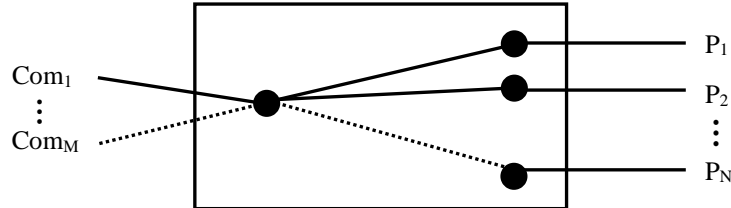


Product: MEMS M (M≤4) × N (N≤128) Optical Switch

Part Number	Spec Number	Version	Date
OPSWXXXXXXXXXXXX	S038	Rev 01	10/30/2021

1 Function Diagram

The 1xN MEMS optical switch is based on a coaxial design where a single MEMS mirror redirects light from a common fiber to one of N ports. At the same time, Triple-Stone can implement multiple Com MxN (M≤4) optical switches in a single device.



2 Specifications

2.1 Environment Conditions

Item	Parameters	Symbol	Min	Typ	Max	Units	Note
1.	Operating Temperature	Top	0		70	°C	
2.	Storage Temperature	Tstor	-40		85	°C	
3.	Operating Relative Humidity	RHop	5		95	%	[1]
4.	Storage Relative Humidity	RHstor	5		95	%	[1]

Note:

[1] Not to exceed industrial standard of 0.024 kg water per kg of dry air under non-condensing conditions.

2.2 Specifications

Item	Parameters	Symbol	Min	Typ	Max	Units	Note
5.	Operation Wavelength Range	λ_{op}	1260 ~ 1670			nm	
6.	Center Wavelength	λ_c	1310 / 1550 / 1625 (By PN)			nm	
7.	Channel Number	CN	By PN			/	
8.	Insertion Loss @ λ_c	IL		1.0	1.5	dB	[2]
9.	Polarization Dependent Loss	PDL			0.15	dB	
10.	Temperature Dependent Loss	TDL			0.4	dB	
11.	Cross Talk	CT	50			dB	
12.	Return Loss	RL	45			dB	[2]
13.	Repeatability	RE	-0.02		+0.02	dB	G
14.	Durability	DU	10^9			Cycles	
15.	Switch Time	ST			20	ms	
16.	Optical Power	Pop			500	mW	G

Note:

[2] Above specifications are with connectors.

G: Guaranteed by design.

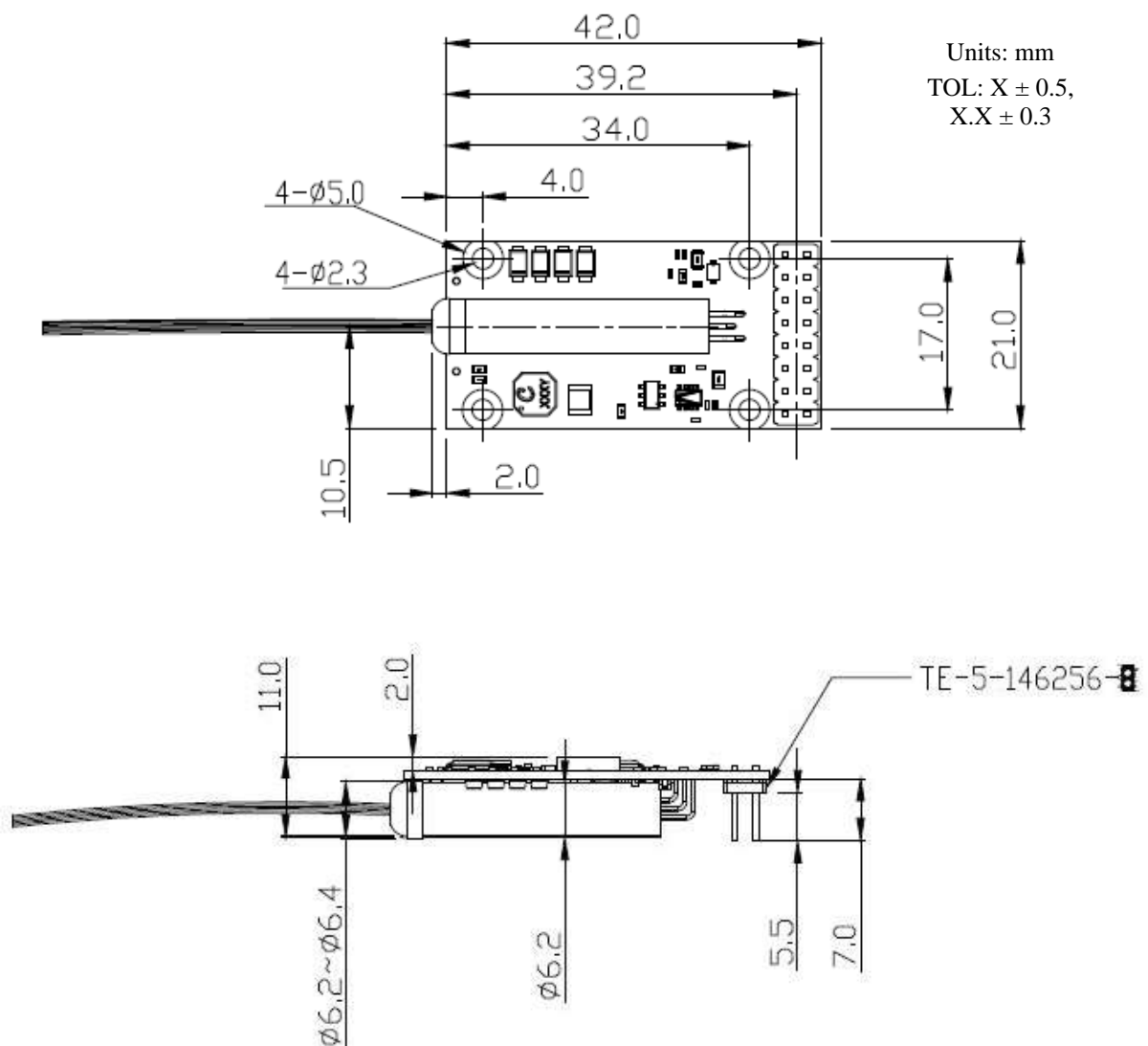
2.3 Mechanical Specifications

2.3.1 Specifications

Item	Parameters	Symbol	Min	Typ	Max	Units	Note
17.	Fiber Type			G657.A2			
18.	Fiber Length			By PN		m	
19.	Fiber Jacket			By PN			
20.	Package Dimension			See below for details		mm	
21.	Connector Type			By PN			

Note:

2.3.2 Drawings



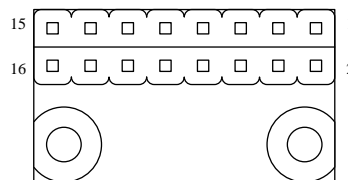
3 Electrical Pin Configuration

Pin	Name	Description	Note
1	TX	USART TX	
2	RX	USART RX	
3~6	NC	No Connect	
7	GND	Ground	
8	VDD	Supply Voltage	[1]
9~12	NC	No Connect	
13	RST	System reset	[2]
14	SDA	I2C SDA (3.3V)	
15	SCL	I2C SCL (3.3V)	
16	GND	Ground	

Note:

[3] The recommended VDD is 5~5.5V. The demanded current f VDD is $\geq 250\text{mA}$.

[4] The system reset will occur when this pin keep the low level long enough. The hold time is advised to be over 4.5ms.



[5] In the pin header, the locations of all the pins are as shown in the figure above. The gap between pins is 2.54 mm.

[6] Please contact our technical staff to obtain detailed communication protocol information.

4 Device Label, Delivery Data

Triple-Stone standard format

5 RoHS

RoHS compliant

6 Order Information

